Overview of the Real Time DPU prototype for space instrument DUSTER

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***Abstract*— This paper proposes an architecture for the data processing unit of the DUSTER instrument for exploration missions to solar system bodies. The DUSTER project objective is to develop instrumentation and technologies for in situ analysis of the charging and cohesion of the dust grain in the oon regolith of the Moon. There are three probes: one shall measure the electric field generated by the dust particles; the second measures the status of the plasma in the surrounding near the regolith and the third analyses the movement of the grains measuring the current resulting from the impact of the charged grains onto the electrodes with high voltage (thousands) applied.**

The DUSTER project is funded by the European Commission with BIRA-IASB leading the project and IAA-CSIC, ONERA and THALES as partners. IAA-CSIC is developing the electronics required to acquire in real time the data from the probes, process it and send it back to Earth for post-analysis. We approach to the development of the instrument from the point of view of a model-based design to address the complexity associated with development of space projects.

The DUSTER hardware platform, prototyped on a Field Programmable Gate Array and relying on the GRLIB IP Library, is designed such that it can be a candidate for qualification and use in future ESA, NASA or JAXA missions, which cannot rely on high performance COTS technologies. In particular, the platform is targeted to be a mixed-criticality platform, allowing the deployment of the instrument in different levels of criticality.

Keywords—DUSTER, FPGA, LEON3

I. INTRODUCTION

A. *DUSTER*

International scientific and commercial interests in exploration missions to solar system bodies such as the Moon, asteroids and comets have increased significantly during the last two decades and will continue to increase in the future. One major environmental constraint during exploration missions is the presence of charged dust-like particles that can be a threat for both human and robotic exploration missions.

The DUSTER (for DUst Study, Transport, and Electrostatic Removal for exploration missions) project aims to analyse the effects of dust adhesion to any type of equipment (e.g. astronauts, rovers, landers and scientific equipment). DUSTER is part of a UE funded project [1] with BIRA-IASB [1] leading the project and TAS-E [2] (THALES Spain), ONERA[3] and IAA-CSIC[4] as partners. BIRA-IASB is coordinating the project and developing the instrument front-ends and provide the high-power supplies of the instrument. IAA-CSIC is in charge of developing the tools (software and electronics) required to acquire the data, process it and send it back to Earth for post-analysis (Electrical Ground Support Equipment, EGSE, data processing unit, DPU, breadboard architecture and the low-voltage power supplies of the instrument). TASE will run EMC tests of the integrated instrument. ONERA is in charge of developing the system (around Technology Readiness Level 4, TRL4) that will charge the dust, activate their transport and measure the generated current and thus the net charge.

The DUSTER instrument shall answer the key questions: what voltage and what type of electrodes are needed to remove the dust depending on the dust properties and the environment (UV, plasma, E-field). The DUSTER instrument uses the High- and Low- voltage power supplies to transport the dust to the probes. Then it detects the current carried by dust grains when they collide with an electrode equipped with high sensitive current amplifiers. From the literature, the charge carried by a single grain is in the order of a few fC up to a few tens of fC and can be mobilized over a few (tens of) centimetres ([2], [3], [4], [5]). Dust charge monitoring is performed with a charge amplifier connected to the output of a Faraday cup (FC). When a dust grain enters the FC, its charge generates a displacement current in the order of the carried charge divided by the dust velocity. The dust velocity itself depends on the dust charge, on the electric field and on the acceleration zone.

B. *Instrument Description*

The DUSTER instrument measures the dust properties and the environment (ultraviolet, plasma, electric field) with three probes: E-Field, DUST and Langmuir. The Low-Voltage

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Power Supply (LVPS) and the High-Voltage Power Supply (HVPS) generate an electric field that transport the dust to the instrument probes. The data processing unit (DPU) manages the probes and the power supplies to perform the acquisition, process the acquired data and generates science and housekeeping telemetries.

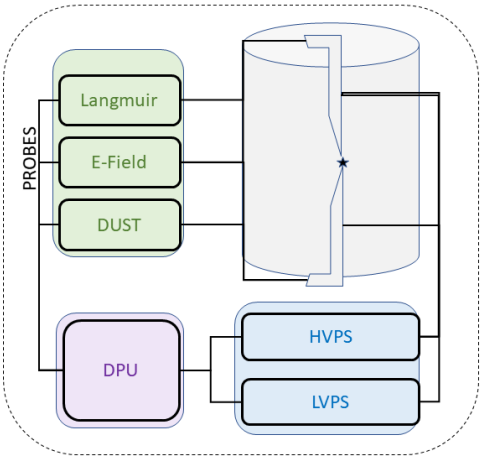

Figure 1 DUSTER Instrument block diagram

Each of the probes has its own front-end that abstracts the management of the analog to digital converter (ADC) and is configured using a serial peripheral interface (SPI).

- The Langmuir probe acquires the current measured by the probe when it operates in sweep, fixed bias and current monitoring mode, as well as the potential of the probe (it monitors the applied bias) in bias monitoring mode.
- The E-Field probe measures the electric field in nominal mode and the voltage provided by the digital to analog converter (DAC) in monitoring mode.
- The Dust probe measures the current acquired by the probe in nominal mode, the current provided by the DAC in current monitoring mode and the voltage applied to the probe (by the HVPS and the ADC) in potential monitoring mode.

The high-voltage power supply (HVPS) receives commands and transmits housekeeping information to the DPU via a serial interface. The output voltage of the HVPS, which is around 5kV, is configurable and shall be adapted to the operation of the DUST probe.

The low-voltage power supply (LVPS) powers the digital components of the instrument and generates the mid-range and low voltages required for the transportation of the dust particles.

The data processing unit (DPU) controls the operation of the probes and the power supplies to perform the science operation, acquires the measurements obtained by the probes, processes them and transmits the results. Moreover, the DPU receives commands with the operation parameters of the instrument.

C. Data production and handling

The operation of the instrument involves transporting dust particles in vacuum environment to the probes and measuring their properties upon collision with a grid. The charged dust particles are attracted to the grid by generating an electric field using the LVPS and HVPS. The instrument will monitor dust counts over several tens of seconds, acquiring data at the highest possible rate to effectively distinguish between consecutive dust particles.

Table 1 Acquisition units for the DUSTER probes

Probe	ADC Sampling (max-min)	DAC	SPI Baudrate
Langmuir	(5kHz-1kHz) / 20 bits	100Hz/16bits	10 - 1 Mb/s
E-Field	1 kHz / 20 bits	1kHz/16 bits	10 - 1 Mb/s
DUST	(10 kHz-1kHz) / 20 bits	1kHz/16 bits	750 – 300 Kb/s

The requirements include both an objective and minimum performance for the acquisition quantities. The allowed data rate for SPI is between 1Mbps and 10 Mbps for the SLP and E-field probes. The DUST probe, because of the high-voltage isolation, data rate is constrained to 300 kbps and 750 kbps. The Langmuir probe must perform bias sweeps with at least 600 steps per sweep and a time resolution of 1 minute, with a goal of achieving 1000 steps per sweep. The E-Field probe will conduct measurements with a time resolution of less than 1 minute. Lastly, dust probe measurements must have a time resolution of at least 10 milliseconds. Table 1 presents the expected acquisition rates of the probes.

II. DUSTER DPU Overview

The DUSTER DPU will execute all software related to instrument management and status monitoring, generating housekeeping data that reflects the instrument's status. It will receive telecommands to adjust the operational parameters of the instrument. The real-time data acquisition task involves the DPU continuously reading the ADC measurements for at least 1 minute. The scientific output of the DUSTER DPU will be a timestamped time series of measurements for both the ambient environment and the dust collected by the probes.

Space systems cannot utilize commercial of the shelf (COTS) processors because they are not designed to support radiation and do not meet qualification requirements. Current space missions often incorporate powerful radiation-hardened ASIC processors[6][7], such as the GR712RC and GR740 from Frontgrade Gaisler. However, while these ASICs include the most common interfaces used in space missions, they lack the flexibility needed to adapt to the specific requirements of the DUSTER project.

In contrast, the soft processors LEON3[8] and NOEL-V[9] are implemented as synthesizable soft intellectual property (IP) cores, allowing for customization and deployment in field-programmable gate arrays (FPGAs). The LEON3 processor, in particular, has been successfully used in various space missions, demonstrating its effectiveness and reliability in harsh environments[10].

The DUSTER DPU is a dual-core system based on the LEON3 processor, which adheres to the SPARC v8 architecture and is built using the GRLIB GPL v2023.2[11]. The GRLIB IP Library, developed by Frontgrade Gaisler, is a comprehensive suite of reusable IP cores designed for system-on-chip (SoC) development. Its primary infrastructure is available as open-source under the GNU GPL license, promoting accessibility and innovation.

A notable feature of the LEON3 processor is its fault tolerance capability against Single Event Upsets (SEUs), particularly in its radiation hardened version, LEON3FT

(Leon3 Fault Tolerant). This fault tolerance mechanism is primarily aimed at protecting on-chip RAM blocks used for IU/FPU register files and cache memory. However, it's important to note that some cores and configurations are exclusive to the commercial version of GRLIB, and the LEON3FT is only available in the fault tolerant (FT) and FT-FPGA versions.

One key advantage of the GRLIB IP Library is its vendor independence, allowing compatibility with various CAD tools and target technologies. This flexibility facilitates seamless integration within model-based development workflows, where projects are constructed using models to represent subsystems and elements rather than relying solely on traditional documentation.

In summary, the DUSTER DPU takes advantage of the capabilities of the LEON3 processor and the versatile GRLIB IP Library, provides a solid foundation for advanced SoC development focused on reliability and integration.

III. Architectural Configuration

The DUSTER instrument is currently under development and therefore changes to the current configuration are expected and will have to be adapted to changing requirements as they arise during development. The development of the different elements of the instrument is being done in parallel and several releases have been scheduled for integration and verification. Once the software and the probes are integrated and the instrument is fully functional, the final platform configuration could be determined.

The baseline configuration of the platform consists of a dual-core Leon3 processor with a system clock of 100MHz. Each CPU features private L1 caches for instructions and data, with 16KB size and 16 bytes cache line length. The L2 cache is disabled. The processor is connected to the debug support unit which is accessible using the JTAG (Joint Test Action Group) and UART (Universal Asynchronous Receiver Transmitter) debug links.

The design includes two memory controllers, one to manage the non-volatile flash memory and the other for the DDR4 volatile memory devices included in the platform. The flash memory is used as permanent storage for the software and firmware of the FPGA. The DDR4 memory is used as the main processor memory for the software execution. Additionally, communication interfaces such as SPI and UART facilitate data exchange with the probes and communication with the control unit. Finally, the Timer Units, Interrupt Controller and General Purpose Input Output (GPIO) controller peripherals, are included in the design to enhance functionality and performance of the system. All these peripherals will be implemented as IP Cores and are provided by the GRLIB IP library. The block diagram of the DUSTER DPU with its main elements is represented in Figure 2.

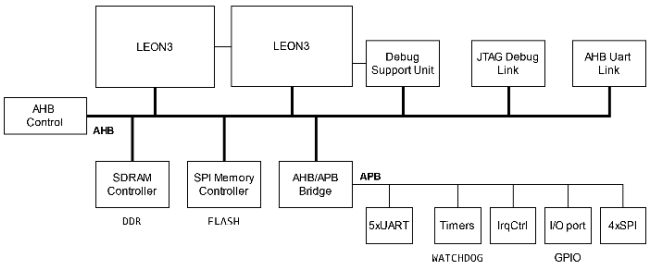

Figure 2 DUSTER DPU block diagram

The SPI interfaces facilitate communication with the probes, with three independent SPI interfaces in the instrument—one for each probe. This design ensures that each probe could meet its timing constraints. The DAC of the probe is also configured using this interface.

Additionally, two UART interfaces connect to the Low-Voltage and High-Voltage power supplies. These interfaces are essential for configuring the power supply outputs, thereby generating the electric fields necessary for observation.

The DPU receives telecommands through one of the UART interfaces, which includes configuration parameters for the instrument's operation. This same interface is also used to transmit housekeeping data and telemetry related to the instrument's products.

Finally, there is an additional UART interface dedicated to logging purposes.

IV. FPGA Device Trade Off

The DUSTER DPU will be prototyped on an FPGA, targeting an architecture suitable for future institutional space missions. To develop the prototype, a large FPGA is necessary to accommodate a multicore system along with the required peripherals and numerous I/O ports. Table 2 summarizes the hardware resources of the most common space FPGAs.

Table 2 Rad-Hard FPGA resources

	LUTs (k) / Flip Flops (k)	**I/O ports**
Xilinx XQRKU060	331/663	620
NanoXplore NG-LARGE	137/129	740
Microchip Axcelerator	21/21	198
Microchip RTG4	151/151	720

We opted not to consider RadHard FPGAs due to their higher cost and the project's low Technology Readiness Level (TRL4). However, we aim to stay as close to RadHard specifications as possible.

The Xilinx XQRKU060 FPGA[12], radiation testing has confirmed that the FPGA is suitable for all orbits, including deep space exploration. The QMLB and QMLY-grade version of the XQRKU60 device could be procured for the final hardware prototype. Furthermore, the Xilinx Kintex UltraScale family[13] includes the XCKU060 FPGA, which is a commercial-grade FPGA, but can serve as a basis for understanding the architecture and capabilities of the XQRKU060. Table 3 presents the hardware resources of the Xilinx UltraScale devices.

Table 3 Xilinx UltraScale family resources

	XCKU040	XCKU060	XQRKU060
Radiation Hardness	None	None	Tolerant
System Logic Cells (K)	530	726	726
CLB Flip-Flops (K)	448	663	663
CLB LUTs (K)	242	331	331
DSP Slices	1920	2760	2760
Block RAM (Mb)	21.1	38.0	38.0
Gb/s Transceivers	20	32	32
I/O Pins	520	624	620

The use of commercial-grade FPGAs offers several advantages, including availability of development boards like the GR-VPX-XCKU060 and GR-CPCIS-XCKU from Frontgrade Gaisler, as well as the ADA-SDEV-KIT3 from Alpha Data. In addition, the Xilinx KCU105 Evaluation Kit, featuring the Xilinx Kintex UltraScale XCKU040 FPGA, provides a robust platform for development.

Additionally, from a firmware development perspective, prototyping for any device in the Xilinx Kintex UltraScale family is effectively the same as prototyping for the XCKU060. The Kintex UltraScale family shares a common architecture, meaning that the underlying hardware resources—such as logic cells, DSP blocks, and memory interfaces—are similar across devices. This consistency allows the usage of a full commercial development board, simplifying procurement and reducing costs.

Prototyping on the Kintex UltraScale XCKU040 device provides a reliable reference for the XQRKU060. The Xilinx KCU105 Evaluation Kit allows to prepare the testing, validation and verification at early stages of the project.

Furthermore, the broader ecosystem surrounding the Kintex UltraScale family, including community resources, forums, and documentation, provides extensive support for developers. This shared knowledge base can be leveraged across different devices, further simplifying the development process.

V. SOFTWARE SUPPORT

The LEON3 architecture is supported by the real-time operating system RTEMS [14] which is pre-qualified for space applications[15]. The prequalification toolkit allows end-users to qualify their space applications. That reduces both the cost and the effort of the development and qualification.

VI. SYNTHESIS RESULTS

The initial step of this DUSTER project involves synthesizing the design shown in Figure 2, followed by benchmarking and analysing its compliance with real-time requirements of the instrument.

We prototyped for the Xilinx KCU105 Evaluation Kit for this synthesis and the actual occupations of the FPGA in terms of slice registers (mostly Flip Flops), combinational logic blocks (CLBs) and the global numbers of occupied I/O is presented in Table 4.

Table 4 Device Utilization Summary.

KCU105 Board	**Occupied resources**	
CLB	9373 of 30300	30%
LUT as Memory	1805 of 112800	1.60%
LUT Flip Flop	15227 of 242400	6.28%
Block RAM	74 of 600	12.33%
DSPs	11 of 1920	0.57%
I/O	221 of 520	40%
GLB CLK BUFF	13 of 480	2.71%

Considering the current state of the project development, the resource utilization of the FPGA design seems adequate, enabling us to continue advancing without concern that any new requirements may render development on this platform unfeasible.

VII. RESULTS AND DEVELOPMENT STATUS

In this short paper, we describe the development of the Data Processing Unit for the DUSTER instrument, designed to analyze dust during special exploration missions. We detail the design of the DPU, which is based on a LEON3 processor and utilizes the GRLIB IP library, while exploring FPGA options for prototyping. We present the architecture and design synthesis results, along with the current status of project development.

The DPU will handle all software related to instrument management and status monitoring. This software must be robust and reliable to ensure mission success. Additionally, the DPU must manage the high data acquisition rates from the three instrument probes and process and transmit this data in real time.

We also emphasize the importance of using a model-based development flow manage the complexities of space projects. Selecting the right FPGA is crucial; factors such as cost, availability, radiation resistance, and compatibility with development tools must be considered. Utilizing the GRLIB IP library—comprising a comprehensive set of reusable IP cores designed for system-on-chip (SoC) development—offers advantages due to its vendor independence and compatibility with various CAD tools and target technologies. This flexibility facilitates integration into model-based development workflows.

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